Novel Technique to Reduce Leakage Current and Commutation Losses in Electric Drives

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Abstract — The continuous advancements in the solid state device engineering the switching transients have been minimized considerably for power switches. They are gaining popularity because of lower switching losses for hard switched systems. However this introduces high leakage current in electric drives. A technique to simultaneously reduce the leakage current while reducing the switching losses is presented in this paper.

I. INTRODUCTION

The EMI aspect is rarely taken into account at the conception of Electric Drives which increases the cost and time to market of the drive train due the tedious and tiresome process of EMI suppression. The problem of common mode current or leakage due to the capacitive coupling between the stator winding and the stator frame along with high 'dv/dt' in the windings give path to non negligible currents (5A) for switching transients of 200ns for DC link voltages as low as 200V. The recent trend of using high speed switches has only worsen the situation. In this paper we present a novel technique of reducing the leakage current as well as the switching losses.

A. Leakage Current

High frequency model of an electrical machine shows a capacitive coupling between the stator end windings and the stator body [1]. Since the stator is connected to the protective earth the current leaks into the earth therefore also called common mode current. These are the main cause of the radiated noise [2]. The expression for the leakage current is given by (1.1) where Cws is about a few nF for well constructed machine while 'dv/dt' is about 5G V/s.

$$I_{leakage} = c_{ws}\frac{dv}{dt} \qquad (1.1)$$

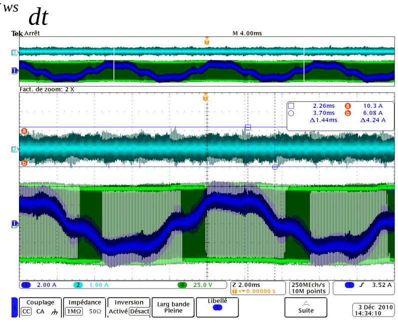

Fig. 1: Leakage current (top), Ia and Va0

Fig. 1 the curves in green and navy blue are the phase voltage and current respectively while the curve in blue on top is the leakage current as observed. The density of the leakage current depends on the modulation frequency f_{PWM}, pulse positioning technique and the modulation technique used. The modulation frequency determines how frequently the voltage commutations occur, the pulse positioning gives the no. of voltage commutations for line voltage, e.g. for pulses placed at the extremes of the modulation period the line voltage has the same no. of voltage commutations as the phase voltage while for pulses placed around the centre of the modulation period give twice as many voltage commutations as the phase voltage whereas the type of modulation technique could alter the effective modulation frequency such as in the case of DPWM techniques.

B. Switching Losses

In Voltage Source Inverters the phase voltage generated has only two levels $V_{dc}/2$ and $-V_{dc}/2$ with respect to the DC mid point and since they both have the same absolute value it becomes a constant while calculating the switching losses hence the only variable then is the phase current [3]. (1.2) gives the switching losses over the fundamental period for a phase.

$$P_{sw} = P_{sw}^{on} + P_{sw}^{off}$$

where,

$$P_{sw}^{on} = \frac{f_{sw}V_{dc}t_{rise}}{2}\frac{1}{2\pi}\int_0^{2\pi}|i(t)|dt$$

$$P_{sw}^{off} = \frac{f_{sw}V_{dc}t_{fall}}{2}\frac{1}{2\pi}\int_0^{2\pi}|i(t)|dt \qquad (1.2)$$

IGBT special case: We seldom take into account the effect of out of phase currents (lagging or leading) which necessitate the free wheeling diodes to continuously conduct for several commutation periods when the phase voltage and currents are of opposite polarity as IGBTs block reverse current (unlike MOSFET). This means there are no commutation losses during this period. In this paper we use this phenomena to our advantage i.e. slow down the switching speed of the IGBT to reduce 'dv/dt' considerably and in turn common mode current and EMI associated to it.

II. DSVM & MODULAR GATE RESISTANCE

Discontinuous modulation techniques abbreviated as DPWM [4] are the modulation techniques valid for poly-phase loads with a floating neutral i.e. it is not tied to the ground. The principle of such techniques is to focus on the line voltages rather then phase voltages as its the potential difference between the phases that matters finally. In this section we have used an evolving discontinuous modulation technique with variable switching transients keeping in mind the continuous conduction period of anti-parallel diodes as explained in the previous section.

A. DSVM

DSVM refers to the modulation techniques that use space vector calculation however the completion of the period using the zero vectors or the sequence of application of the vectors changes to achieve voltage clamping essentially done to decrease the switching losses. The most basic DSVM techniques could be achieved using only one of the two zero vectors at a time which is analogous to DPWMmin and DPWMmax if V_0 or V_7 is used respectively [5]. A simple yet very effective algorithm Fig. 2 is developed to reduce the switching losses as much as possible using (1.3) to clamp a given inverter leg.

$$T_{a\_clamping} = \begin{cases} x, & for\ \frac{\pi}{6} \le \omega t < \frac{2\pi}{3} + \frac{\pi}{6}, \\ & or \\ x - \frac{2\pi}{3}, & for\ \frac{\pi}{6} + \pi \le \omega t < \frac{2\pi}{3} + \frac{\pi}{6} + \pi \end{cases}$$
$$where\ x \in \left[0, \frac{2\pi}{3}\right] \quad (1.3)$$

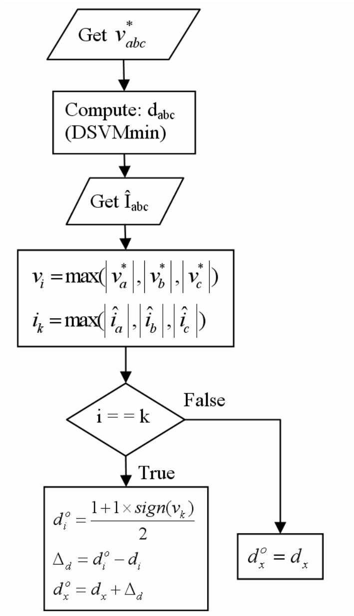

Fig. 2: Algorithm DSVM

A different dead time correction algorithm is used with this technique. The duty cycles are re-adjusted to compensate the slower commutations, for extreme values (around 0 or 100) of duty cycle there is less margin for the compensation hence lesser liberty to slow down the switching. Fig. 3 shows a reduction in the switching losses, the leakage current magnitude and its density for a modulation index of 0.907. The drop in the Il reduction around 60° is due to the presence of the third harmonic component in the phase voltage. Only the first quadrant is shown as the curve is symmetric about φ=90°.

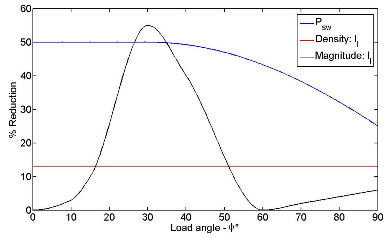

Fig. 3 : Switching losses and leakage current magnitude and desity reduction

III. EXPERIMENTAL SETUP AND RESULTS

The test bench consists of two electric motors mechanically coupled fed by two different inverters controlled independently. One electric drive emulates a variable load to perform different driving cycles and the other drive under observation consists of a 15 kW, 3-phase 2-level IGBT inverter fed by an adjustable DC link and a 3 kW PMSM with an incremental encoder (4096 points).

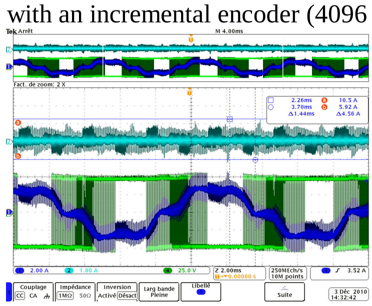
Fig. 4: DSVM Leakage current (top), Ia and Va0

In Fig. 4 the green curve shows the voltage clamping at high current (navy blue curve) values and its affect on the leakage current (blue curve) density, its very sparse compared to Fig. 1. As expected we see that at higher switching frequency the losses are further reduced which means while the conduction losses remain constant the switching losses increase with increase in frequency.

F_{PWM} (kHz)	Loss reduction (%)
15	12.98
25	20.75
35	22.82

Global inverter losses are calculated measuring the power supplied by the DC link and comparing it with the power at the inverter legs for the proposed and the standard technique. The experimental results show a decrease in losses from 7.18% to 5.69% which translates to an overall reduction of 20.75% for a switching frequency of 25kHz. Current density reduced by 17% with smaller peaks around phase current zero crossing.

IV. REFERENCES

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